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A monolithically integrated surface micromachined touch mode capacitive pressure sensor

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Abstract

A monolithically integrated surface micromachined touch mode capacitive pressure sensor and its interface circuits are presented. The device includes the capacitance to voltage, and capacitance to frequency converters on the same chip. The sensor is fabricated using a surface micromachining technology, which is processed simultaneously with a conventional 2.0-μm double-poly, double-metal n-well CMOS process. The performance of the integrated sensor meets the design specifications of good linearity and good stability. Evaluation results on the completed 'sensor and circuit' chip are presented. © 2000 Elsevier Science S.A. All rights reserved.

Keywords: Integrated sensor; Capacitive pressure sensor; Touch mode; Capacitive sensors; Surface micromachining technology; CMOS

1. Introduction

Capacitive pressure sensors have been developed for industrial applications for many years with advantages of high sensitivity, low temperature drift, robust structure and low sensitivity to environmental effects [1,2]. However, the output capacitance of microsensor is normally very small (the order of fF or pF) and is very susceptible to parasitic effects [3]. In order to detect such small capacitance changes, a well-matched readout circuit is required and it has to be placed as close as possible to the sensor. Therefore, on-chip integration of sensors with interface circuits is important in this application. Surface micromachining is a promising technology to achieve this goal. Nonlinear characteristics is another drawback of the normal mode capacitive sensors. Much effort has been made to improve the linearity of capacitive sensor either by modifying the structure of sensors or by designing special interface circuits [4–7]. Among those attempts, touch mode capacitive pressure sensor is a promising design to fabricate a linear capacitive sensor with a simple structure [8]. Touch mode capacitive pressure sensors are intentionally designed to operate in the range where the diaphragm touches substrate. The change of capacitance is mainly determined by the touched area, and is proportional to the applied pressure [9]. The advantages of touch mode capacitive pressure sensor are good linearity near the operating point, large operating pressure range, large overload protection, and zero suppression possibility.

In this report, we present a prototype of a touch mode capacitive pressure sensor integrated with CMOS interface circuits. The fabrication of the prototype combines two technologies: surface micromachined sensor fabrication process using polysilicon as the diaphragm, and conventional 2.0-μm double-poly, double-metal n-well CMOS IC process for the interface circuits.

2. Design and fabrication process

2.1. Design of the sensor element

The plan view and cross-sectional view schematic drawings of a circular micromachined sensor element are shown in Fig. 1. The sensor consists of a polysilicon deformable diaphragm with thickness h, referred to as the top electrode, and a polysilicon layer covered by an insulating layer, t on an isolated silicon substrate, referred to as the bottom electrode. The two electrodes are separated by an initial gap, d. The top electrode is formed using an in situ phosphorous doped polysilicon layer and its dimension can be precisely controlled. The bottom electrode is formed during CMOS gate definition, thus saving one photolitho-

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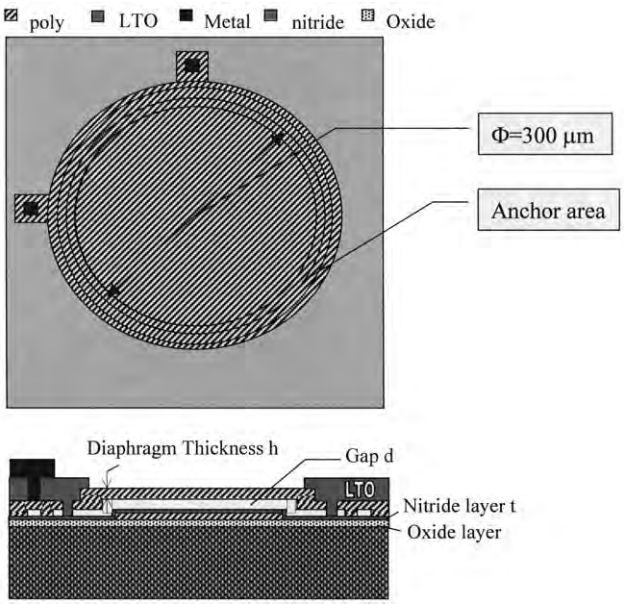

Fig. 1. The plan view (a) and cross-sectional view; (b) schematic drawings of a circular surface micromachined sensor element.

graphic step for the total process. The vacuum reference cavity formed between two polysilicon plates is hermetically sealed with LTO in low vacuum (20–30 mTorr), thereby creating an absolute pressure-sensing device. To fabricate the sensor structure, three photomasks are used in addition to the masks used in the conventional double-poly CMOS process. The parameters (h, t, Φ and d) of the sensor structure are determined by a mechanical simulation program [10] and the output characteristics of the sensor are also computed with this program.

2.2. Interface circuit configuration

A diagram of the dual output capacitance interface circuit is shown in Fig. 2. It consists of four parts: a capacitance-to-current converter (C/I), a three-phase clock generator, a current to voltage convert (I/V) and a current-to-frequency convert (I/F). The operation principle of the C/I converter is described in Fig. 3a. The circuit is controlled by a three-phase non-overlapping clock. During

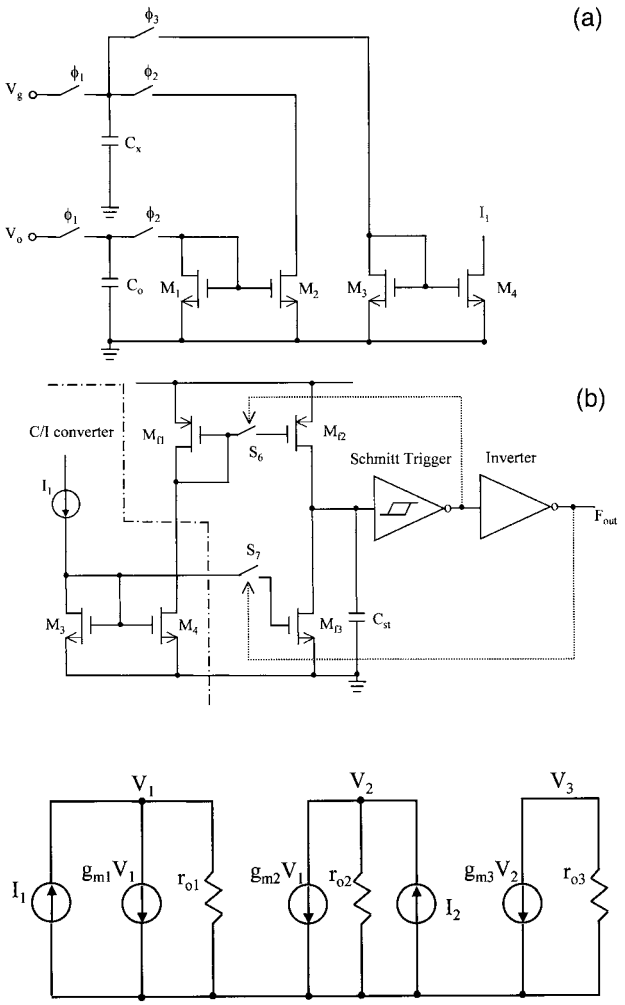

Fig. 3. The electrical circuit diagrams of (a) the capacitance-to-current converter; (b) the current-to-frequency converter; (c) current difference to voltage converter; (d) small signal equivalent circuit of current difference to voltage converter.

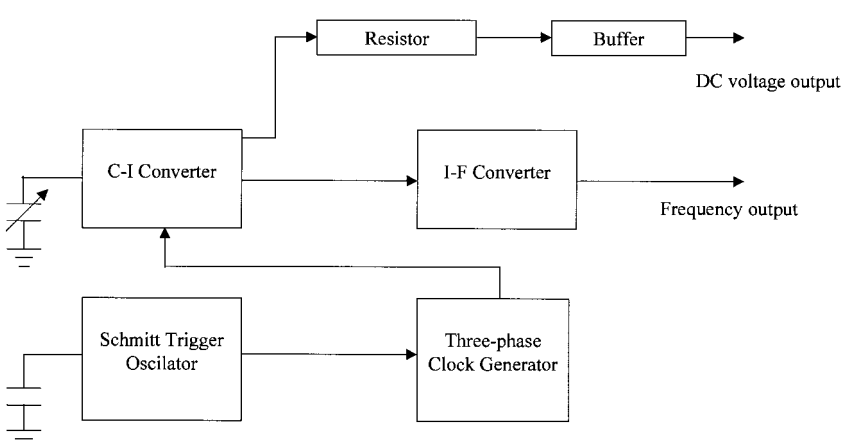

Fig. 2. The block diagram of dual output (C/F, C/V) interface circuit system.

phase 1 (ϕ_1) C_x and C_0 are charged to V_g and V_0, respectively, assuming $(V_g C_x - V_0 C_0) > 0$. Here, V_0 together with C_0 is used to adjust reference or offset output, while V_g is used for gain control of the C/I converter. During phase 2 (ϕ_2), the charge in C_0 is discharged through M_1. The same amount of charge will be drawn from C_x through M_2 in the same period. The charge remaining on C_x at the end of phase 2 is:

$$Q = V_g C_x - (V_0 - V_T) C_0. \quad (1)$$

Where V_T is the threshold voltage of M_1 and M_2. In phase 3 (ϕ_3), the charge left in C_x discharges through M_3. If the process repeats at the cycling clock frequency, the average current, I_1, sensed at right hand of the current mirror (M_4) is [11]:

$$I_1 = f\left[(V_g - V_T) C_x - (V_0 - V_T) C_0\right]. \quad (2)$$

Here, it is assumed that the threshold voltage V_T of M_1, M_2, and M_3 are the same. Hence, the change of C_x can be represented by the change of current I_1 flowing through the transistor M_4.

The I/F converter is used to convert current to frequency, its operation principle is described in Fig. 3b. The conversion is implemented by a Schmitt trigger together with a charge current source and a discharge sink [12,13]. The Schmitt trigger has two trigger points, i.e., high threshold voltage, V_H, and low threshold voltage, V_L. When the voltage on C_{st} is less than the V_L, the output of the Schmitt trigger is high, thus the output F_{out} is low. The high output signal of the Schmitt trigger turns S_6 on, the current through M_{f2}, which is equal to the mirrored current, I_1 from C/I converter, will charge C_{st} until its voltage reaches the V_H. At this time, the Schmitt trigger toggles. The output of the Schmitt trigger becomes low and output F_{out} becomes high. The high output signal F_{out} turns on S_7, the capacitor C_{st} is discharged through M_{f3}. The discharge current is also the mirrored current, I_1. The charging and discharging time are the same, which is equal to $V_c C_{st}/I_1$. Thus, the output frequency can be expressed as:

$$F_{out} = \frac{I}{2V_c C_{st}} = \frac{f\left[(V_g - V_T) C_x - (V_0 - V_T) C_0\right]}{2V_c C_{st}}, \quad (3)$$

where V_c is the threshold voltage of the Schmitt trigger, which is the difference between V_H and V_L.The resolution of the converter can be expressed as:

$$\Delta F_{out} = \frac{f(V_g - V_T)\Delta C_x}{2V_c C_{st}}. \quad (4)$$

The voltage output can be obtained from the converted current I_1 in the C/I converter using an R-circuit shown in Fig. 3c. The converted current I_1, can be used as the first inputs of R-circuit. I_2 can be generated using another C/I converter by replacing C_x and C_0 with C_f and C_{fo} and $V_g = V_0 = V_3$. The stray capacitance in C_f' and C_{fo} are the stray capacitance of the wiring layout in ''R'' circuit. It is not determined but it is compensated by the 2nd current mirror circuit, so that $C_f = [C_f' + C_{strayf'} - C_{strayfo}]$. According to the Eq. (2), the current I_2 in Fig. 3c can be obtained as:

$$I_2 = f(V_3 - V_T)\left(C_f' + C_{strayf'} - C_{strayfo}\right) = f(V_3 - V_T) C_f. \quad (5)$$

The simplified equivalent small signal circuit for the R-circuit is shown in Fig. 3d, where g_{mi} and r_{oi} are the transconductance and output resistance of the ith MOSFET, respectively. From the small signal circuit, we have,

$$V_1 = \frac{r_{o1} I_1}{1 + g_{m1} r_{o1}} \quad (6)$$

$$V_2 = (I_2 - g_{m2} V_1) r_{o2} \quad (7)$$

$$V_3 = V_2 g_{m3} r_{o3} = \left(I_2 - \frac{g_{m2} r_{o1} I_1}{1 + g_{m1} r_{o1}}\right) r_{o2} g_{m3} r_{o3}. \quad (8)$$

When $g_{m1} = g_{m2}$ and $g_{m1} r_{o1} \gg 1$, then

$$V_3 = (I_2 - I_1) r_{o2} g_{m3} r_{o3} = (I_2 - I_1) R \quad (9)$$

where $R = g_{m3} r_{o2} r_{o3}$. From Eqs. (2) and (5), we have:

$$V_3 = R\left[f(V_g - V_T) C_x - f(V_0 - V_T) C_0 - f(V_3 - V_T) C_f\right]. \quad (10)$$

By solving Eq. (10), the output voltage V_3 of the R-circuit can be written as:

$$V_3 = \frac{R\left[f(V_g - V_T) C_x - f(V_0 - V_T) C_0 - f(V_3 - V_T) C_f\right]}{1 + fRC_f} \quad (11)$$

If $fRC_f \gg 1$ then

$$V_{out} = V_3 = \frac{V_g C_x - V_0 C_x - V_T(C_x - C_0 + C_f)}{C_f} \cong \frac{V_g C_x - V_0 C_0}{C_f}. \quad (12)$$

The output of the C/V converter is independent of the clock frequency. C_M is a capacitor used to filter away high frequency current ripple in output.

The sensitivity of the converter is defined as:

$$S_{C_x} = \frac{\partial V_{out}}{\partial C_x} = \frac{V_g - V_T}{C_f}. \quad (13)$$

The sensitivity of the C/V converter can be adjusted by the voltage V_g or the capacitor C_f.

For optimizing the electronic design and testing the circuit before fabrication, a schematic design is created and simulated using commercial PSPICE software in which the sensor module is treated as a capacitor. After the circuit is optimized, a netlist file is generated for the post-layout vs. schematic check.

2.3. Layout design

The entire microsystem layout is generated using L-edit software. The conventional IC layout is checked by the Orbit 2.0 um CMOS design rule provided by L-edit software. A modified design rule based on the Orbit design rule is added for the inspection of the sensor element layout. The post-layout verification tool, which is used in the IC layout, like netlist extraction for post-layout simulation and layout vs. schematic check, is used for the design verification. In this way, an error-free layout of the microsystem is efficiently generated.

In order to evaluate the characteristics of the proposed technology for the monolithic fabrication of capacitive pressure sensors and interface circuits, a set of demonstrations has been designed. The final layout consists of six dies that include sensors, circuits, sensors combined with circuits, as well as CMOS test structures. Under the same pressure loading, the maximum stress at the edge of the diaphragm is larger for the square diaphragm than the circular diaphragm, when the diameter equals to the length of the square side. So the circular shape of the sensor diaphragm is drawn in the final layout because it has higher overload capacity than a square one. The overall dimensions of the deformable sensor area are 250 and 350 μm in diameter. There are two different interface circuits; a capacitance/frequency converter and a capacitance/voltage converter. The circuit design was shown to be operational through the MOSIS prototyping process before introducing them into this proposed technology. Half of the chips are composed of sensors and circuits in the same die and the other half just the circuits. CMOS test structures contain MOS transistors with different gate widths and lengths, field transistors, capacitors, Kelvin structures, contact resistors, contact chains, inverters, Serpentine/comb resistors, cross-bridge resistors, diodes, and two 31-stage ring oscillators. These structures are used to characterize the CMOS process and extract parameters for PSPICE simulation. The measurements on test chips were used to find if any electrical parameter from the standard CMOS process has changed due to the extra surface micromachining processes, i.e., deposition of Si_3N_4 (820°C), Poly3 (610°C), and PSG(400°C). Since the temperatures in these extra processes are relative low, the changes of the process parameters such as threshold voltage, sheet resistances of P + and N + layers, etc., are very small (less than 5% of the designed values). So their influence on the circuit performance can be neglected.

2.4. Fabrication

The sensor and CMOS electronics were fabricated on 100 mm (100)-oriented, p-type silicon wafers. To obtain the complete microsystem, 15 photolithography steps are used. Among 15 masks, there are 12 masks for the standard 2.0 μm n-well double-poly and double-metal CMOS process. Only three additional masks are used for surface micromachining since the bottom electrode is formed when poly1 is patterned. These three masks are anchor etch, release open, and poly3. Fig. 4a–f gives a schematic representation of the fabrication process steps. When both n-channel and p-channel source/drain implantation and drive-in are done, the standard CMOS process is interrupted and additional surface micromachining steps follow. First, the whole wafer is covered by a 300 nm-thick LPCVD silicon nitride layer, which serves as an insulator between two parallel-plates of the capacitor when these two electrodes touch together. The silicon nitride layer also provides sufficient protection of all CMOS circuits on wafer. A 1.5-μm PSG sacrificial layer is deposited on the silicon nitride and is patterned to define the cavity area. Another 0.5-μm PSG layer is then deposited. Both layers are used as sacrificial material but the latter layer serves as a release path to the cavity. The next mask is printed to define anchor openings where PSG is etched away to anchor the polysilicon structure to the silicon nitride layer. A 2.0-μm LPCVD phosphorous doped polysilicon is deposited at 580°C, followed by an annealing step at 950°C for 30 min, resulting in a sheet resistivity of 20 Ω/□. Since this polysilicon layer is used as diaphragm structures, the intrinsic stress in the film has to be carefully controlled by the process. The release opening is next patterned outside of the cavity area. This means that the gap around the release opening area is about 0.5 μm, so the cavity can be easily sealed by LTO deposition latter on. After the release holes of the polysilicon is etched in a plasma reactor using 1:1 Cl_2:He, the wafer is released by 49% HF for about 10 min. During the release etch, all the CMOS circuits are protected by the 2.0-μm polysilicon plus 0.5-μm PSG and 0.3-μm silicon nitride. Since the etch rate of silicon nitride in 49% HF is about 10 nm/min, the release etching time must not exceed 20 min so that there is enough silicon nitride inside the cavity to isolate underneath electrode. Next step is to pattern the polysilicon to define sensor diaphragm. All the polysilicon outside of the sensor area is stripped by dry etching, followed by a BHF step to remove all the PSG layer on top of CMOS area. The wafers are then cleaned in a standard piranha and RCA procedure, followed by an LTO deposition step. Subsequently, the cavity is sealed by a 1.0-μm LTO layer deposited at a low pressure of 30 mTorr. At this point, all steps for sensor fabrication are done. The wafers continue to be processed to complete the rest of CMOS fabrication, namely metallization steps including contact, metal1, via, metal2, passivation. The wafers are then ready for standard dicing and packaging. It is found that the sealed diaphragm is able to survive the rest of processes including photo resist spin coating. It should be pointed out that there are several critical steps which can alter the device parameters. First, the poly-Si diaphragm of the sensor is covered by a thick LTO ($\sim$ 2.0–2.2 μm) layer, which should be etched away in the contact-etch step and the via-etch step. The

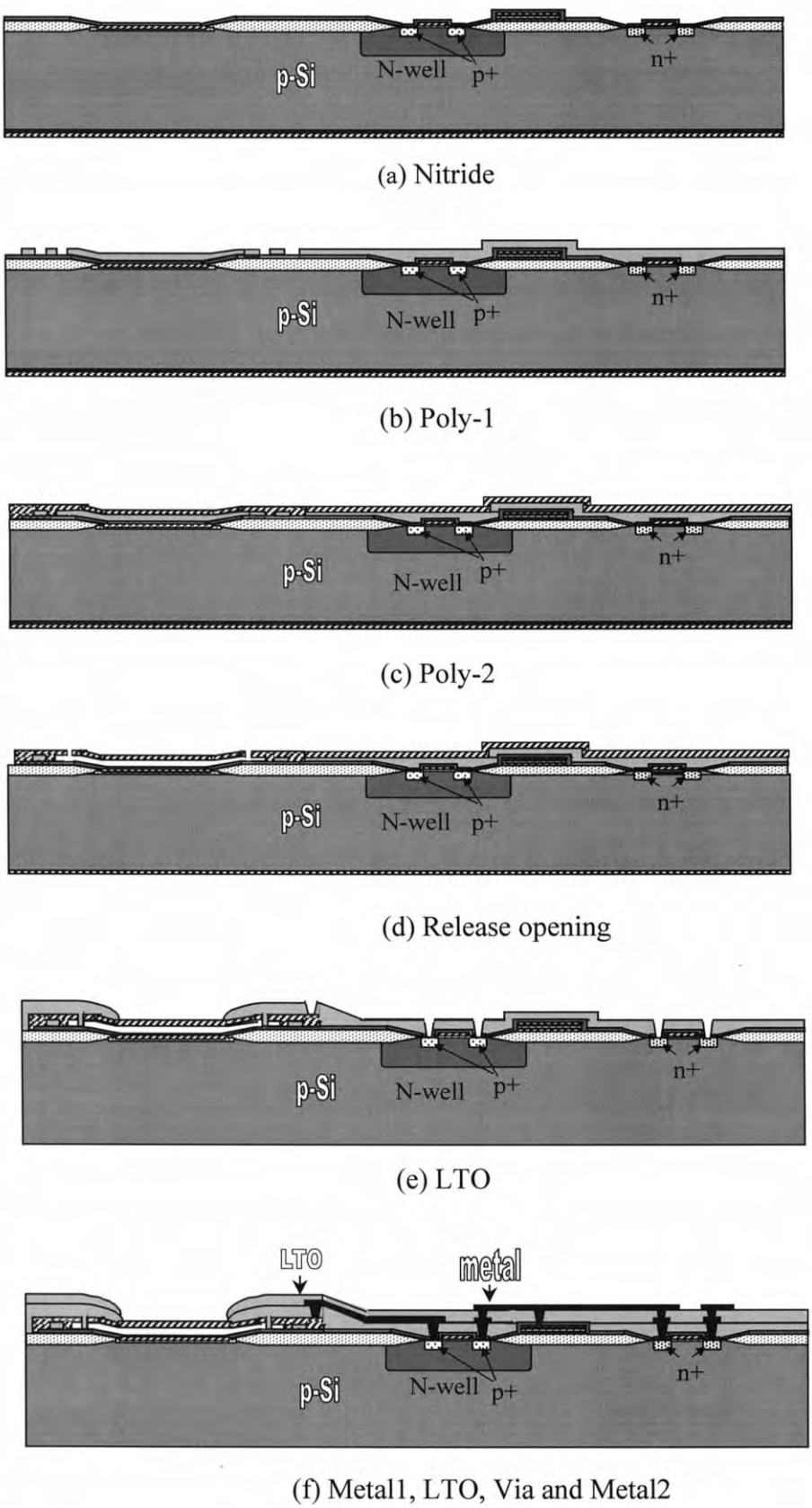

Fig. 4. Schematic representation of the fabrication process of a CMOS integrated surface micromachined touch mode pressure sensor: (a) nitride deposition right after n + and p + source/drain formation; (b) PSG deposition and anchor etch; (c) in situ doped polysilicon deposition; (d) open window and release; (e) LTO deposition and contact open; (f) metal1, LTO, via, metal2.

LTO is etched in CF_4/He with a dry etcher (TEGAL). Since the LTO/poly-Si etch rate ratio is about 3 to 4, the over etch which happens during the dry etch step can change the diaphragm thickness of about 0.1–0.3 μm. The wet etch can well stop at poly-Si layer, but it introduces a lateral etch. Hence for the accurate control of the poly-Si diaphragm thickness, a combination of dry etch and wet etch on LTO is necessary for the best result. Secondly, the film stress and the roughness on both sides of the poly-Si diaphragm are important factors to determine the output properties of the touch mode pressure sensors. Besides, it is also found that a tensile stress in the film is able to avoid sticking problems. Hence, a fine grained, low stress, smooth poly-Si layer is needed for the formation of the sensor diaphragm. In this process, the stress in a 2.0-μm LPCVD polysilicon film deposited at 580°C is found to be smooth with 160–170 MPa in tension. After phosphorous diffusion (875°C, 2 h), the stress is reduced to 25–35 MPa under tensile. Thirdly, during release step, the sacrificial layer is laterally etched from edge to center. The thickness of silicon nitride covered on bottom electrode inside the cavity will vary from center to edge with difference about a few hundred angstroms. It will change the linear output properties of the touch mode pressure sensors.

3. Results and discussion

An optical photograph of a completely processed chip is shown in Fig. 5. The CP11 circuit, which has only frequency output, is on the top-left and the CP12 circuit, which has both frequency and DC output, is on the bottom left. A pair of circular pressure sensors in the left middle of the chip are the sensor capacitor C_x and reference capacitor C_0. Both are connected to the CP11 circuit right above them in the figure. The C_0 has no cavity underneath so it is not sensitive to pressure. Another pair of circular pressure sensors, which are located in the right middle of the chip, are connected to CP12. A test capacitive pressure sensor is on the right center of the chip. After full processing, little damage to the diaphragm (the broken diaphragm is less than 2%) was observed, which indicates that the mechanical strength of the sealed sensor diaphragm is strong enough to survive all the processing steps including photo resist spin-coating. Although some diaphragms may be contacting the bottom plates after LTO sealing, they will not be bonded to substrate because there are no remaining high temperature processing steps after this step. The test result on the completed wafers shows that the fabrication yield of the sensors is up to 80%.

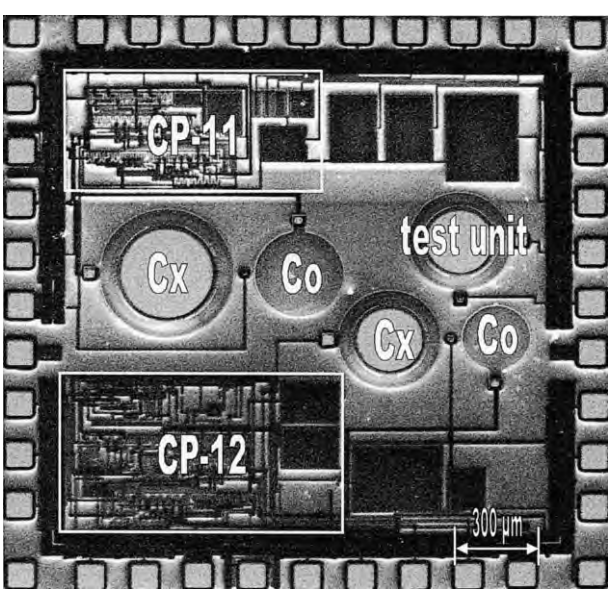

Fig. 5. Photograph of the complete 'sensors and circuits' chip. The single electronic subcircuits are outlined. The sensor element is placed in the middle of the chip.

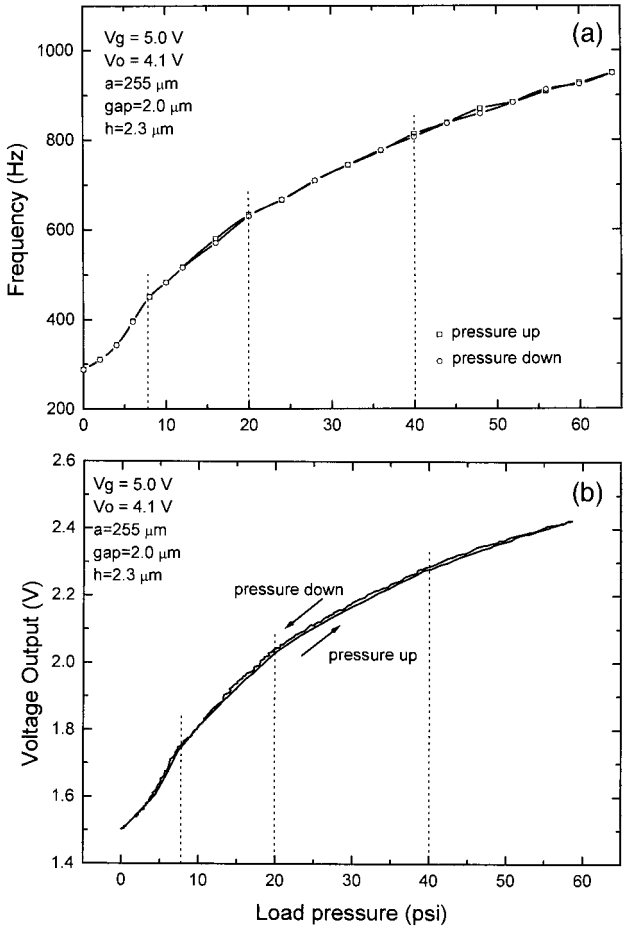

Fig. 6. (a) Measured DC output and (b) measured frequency output of the surface micromachined capacitive pressure sensor integrated with the interface circuit of CP12.

Fig. 6a and b shows the typical frequency and voltage outputs of the converter. The C/V converter is adjusted by varying V_0 to get an offset voltage larger than 1.5 V. The power supply is 4 mW from a 5-V regulated DC source. The control voltage V_g is 5.0 V and V_0 is 4.1 V. The span

of the voltage output can be adjusted by changing the sensitivity of the circuit, normally by shunting an external feedback capacitor. The frequency output also can be adjusted by varying an external capacitor. The non-linearity is defined as:

$$\left\{\frac{|\Delta F_+| + |\Delta F_-|}{2(F_{\max} - F_{\min})}\right\}100\% \quad (14)$$

where ΔF_+ and ΔF_- are the maximum and minimum deviation from the straight line characteristic, respectively. $F_{\max}$ and $F_{\min}$ are the maximum and minimum output frequency in the operating range, respectively. A similar equation can be expressed for the voltage output results.

The typical C–P characteristic of the touch mode capacitive pressure sensor has four regions, i.e., normal, transition, linear and near saturation regions [9]. The linear region and the near saturation region can be used for different applications. In Fig. 6a, the frequency output sensitivities measured in the range of 8–20 psi (the linear region) and 20–40 psi (the near saturation region) are 15.3 Hz/psi and 9.0 Hz/psi, with non-linearity of 0.63% and 0.80%, respectively. In Fig. 6b, the DC output sensitivities are 23.5 mV/psi within a pressure range of 8–20 psi and 12.2 mV/psi within a pressure range of 20–40 psi with the corresponding non-linearity of 1.8% and 1.4%, respectively. The sensitivity can be adjusted by process parameters. The frequency and DC sensitivities obtained from different devices vary from 5.0 to 25.0 Hz/psi, and 10 to 50 mV/psi while the touch point pressure varies from 0 to 8 psig (gauge pressure) or from 15 to 23 psi-ab (absolute pressure). This means variation of $\Delta P_t/P_t = 52\%$ to 35%, which may be caused by variation of poly-Si diaphragm thickness of 13% to 9%, because the touch point pressure P_t is proportional to the fourth power of the diaphragm thickness h, $P_t = kh^4$ (k is a constant) [9]. Therefore, a small amount of the thickness variation across a wafer will lead to a large amount of shift in the touch point pressure.

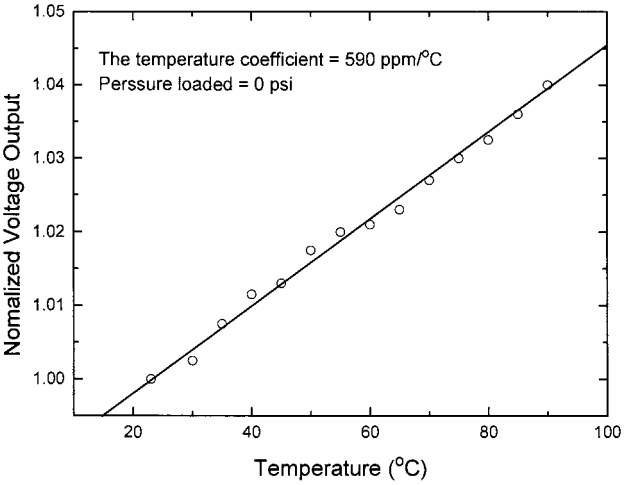

Fig. 8. The zero offset temperature characteristics of the sensor–circuit system.

Fig. 7 shows the comparison of the measured C–P characteristics with the simulated result. The diameter of the sensor diaphragm is 255 μm. The thickness of the diaphragm, the initial gap, and the isolation layer are 2.0, 2.0 and 0.025 μm, respectively. These parameters are used to calculate the C–P characteristics using a spreadsheet solution program [9]. Fig. 7 shows a good agreement between the measured result and simulated result.

Fig. 8 shows the zero offset variation in the temperature range between 23°C and 90°C. The zero offset is the voltage output at zero load pressure. The output voltage is normalized with respect to the output at $T = 23$°C. A temperature-controlled oven with accuracy of ± 0.1°C is used to provide the test temperature ambient. The zero offset temperature coefficient of the entire sensor–circuit system is less than 590 ppm/°C over the entire tempera-

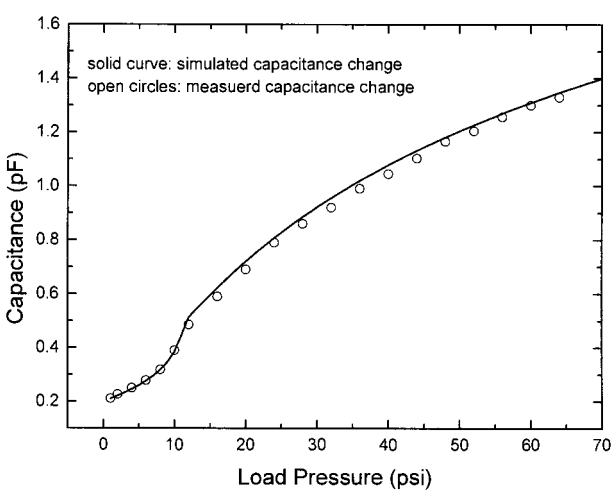

Fig. 7. Comparison of the simulated C–P and the measured C–P characteristics. Diaphragm thickness = 2.0 μm, gap = 2.0 μm, insulating layer = 0.025 μm. The diameter of diaphragm = 255 μm.

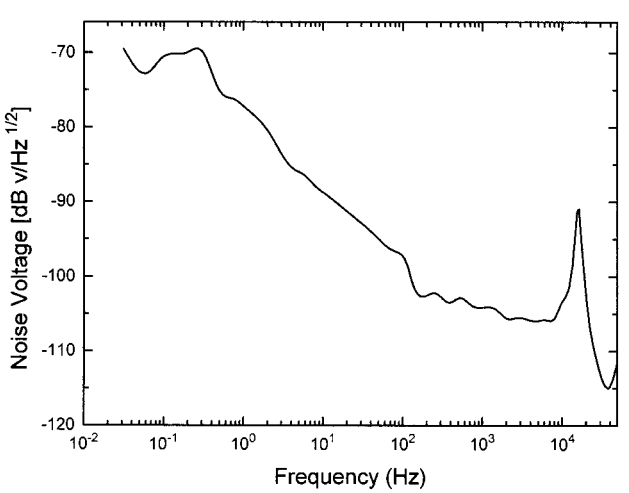

Fig. 9. Noise frequency response curve of CP-12 voltage output circuit, measured at the zero load pressure with an HP 35670A dynamic signal analyzer.

ture range. The temperature characteristics can be improved by adding a temperature compensation circuit. One order of magnitude of improvement is achieved by using a temperature sensitive current source.

The noise of CP-12 voltage output circuit was measured at the zero pressure in a range of 0.03 Hz–50 kHz using a Hewlett Packrad HP 35670A dynamic signal analyser. An external capacitor with value of 1000 pF was connected to the output, which acts as a low-pass filter to limit the output bandwidth to 10 kHz. Fig. 9 shows the measured noise spectrum. The noise is a combination of white and $1/f$ noise, which amount to 210 μV $(\text{Hz})^{-1/2}$ at 0.03 Hz and 2.8 μV $(\text{Hz})^{-1/2}$ at 10 kHz. The peak at around 15 kHz is the property of the ''*R*-circuit loop'' show in Fig. 3c where V_3–I_2–V_3 circuit is a closed loop control unit. The $R = g_{m3} r_{o2} r_{o3}$ and stray capacitors of M_{R2} and M_{R3} cause the frequency respond to peak at 15 kHz. The total noise can be estimated from the square root of the integrated area of noise power spectrum within the defined frequency range. The values of the total noise are 0.36 and 0.39 mV in the frequency ranges of 0.03 Hz–1 kHz and 0.03 Hz–10 kHz, respectively. The value measured with a digital voltmeter with 5 kHz bandwidth was 0.1–0.2 mV rms equivalent. In order to determine the peak-to-peak value of the noise, the output signal was observed over a period of 10 s. The measured peak-to-peak voltage was 0.6 mV, which corresponds to approximately 0.025 psi. Thus, referring to the full-scale output (60 psi), the signal-to-noise ratio is S/N = 67.6 dB.

The long-term stability of the voltage output of the device was tested for 1 week and the baseline drift at constant temperature is less than 1 mV rms, or 0.06% with respect to the mean value of 1.728 V over the continuous test period. The frequency output is also measured at the same time. The variation of the output frequency is ±7.3 Hz, or 0.78% (~ 0.47 psi) with respect to the mean value of 936.0 Hz, which corresponds to 60 psi.

4. Conclusion

We have fabricated and tested a fully CMOS compatible surface micromachined touch mode capacitive pressure sensor. The CMOS interface circuit works properly after integration with the sensors. There is no obvious shift in threshold voltage observed after the additional sensor fabrication process steps are added to the CMOS process for sensor fabrication. Measurement results of the completed sensor and circuit are in good agreement with simulation results. The frequency and voltage output sensitivities are between 5.0–25.0 Hz/psi, and 10–50 mV/psi in the linear pressure range of 8–60 psi. Since the membrane thickness and cavity depth can be very well controlled by the process, the sensors can be designed for different pressure ranges with higher sensitivity, or better overpressure protection. The integrated chip has a total noise of 0.39 mV in the frequency range of 0.03 Hz–10 kHz and long term stability of 0.06% F.S. per week. The power consumption of the total system is less than 5 mW. The technology also allows for inexpensive batch fabrication and integration of sensors with dedicated signal detection circuits. Although stiction at low pressure range may introduce hysteresis, some solution from the literature may be incorporated [14]. With proper package and small modification of structure, the fluid flow, force, acceleration and displacement can be converted into pressure. Therefore, the integrated sensors can be used to measure flow, force, acceleration and displacement in automotive and other industrial applications.

Acknowledgements

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